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Code No: A5706

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November-2011
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Explain about the ALTERA's third generation architecture of MAX7000 family with a neat diagram.
b) Compare the following programmable logic families of ROM, PLA and PAL. [12]

2.a) Explain about Lattice PLSI architecture.
b) Distinguish between FPGA and CPLD. [12]

3.a) Explain how ACTEL ACT2 FPGA family is architecturally close to MPGA. Compare RAM and anti fuse based FPGAS.
b) What are optimized reconfigurable cell arrays? Explain their features and performance. [12]

4.a) Explain about one hot state machine with state table and state diagrams.
b) Explain the advantages of one hot encoding with suitable examples. [12]

5.a) Explain the truth table and state diagram type design entry methods of FPGA Advantage Tool.
b) Explain the FPGA design flow of parallel controller as a case study. [12]

6. Design an 8-bit counter using D flip-flops. Write code for mentor graphic EDA Tool "FPGA Advantage" for this design. [12]

7. Design a digital system which performs a binary multiplication using ASM chart and design the controller of the system. Implement the same using PLA. [12]

8. Write short notes on
a) Meta stability and synchronization.
b) Non-register PLD architectures. [12]

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